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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,853	01/20/2004	Sun-Teck See	3016P	3070

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,853	SEE ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-27 are in the application.

Claims 1-27 are rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2,11-12 rejected under 35 U.S.C. 103(a) as being unpatentable over APA (US Application 10/761853), and in view of Pua et al (US2004/0255054).

As for claim 1, APA describes A FLASH controller comprising: a USB interface unit (Fig 1: #14), wherein USB interface unit implements a USB standard that has a bus speed equal or greater than 12 Mb/s; an internal bus coupled to the USB interface unit (Fig 1: #26); and a FLASH interface unit coupled to the internal bus (Fig 1: #16), the claim further recites the

FLASH interface unit includes FLASH controller logic that allows the throughput for access to a FLASH memory to match the speed of the USB standard. APA does not describe the claim's detail of the controller that matching the throughput of the flash memory. However, Pua describes a controller circuit (Fig 2: #23, #24) capable of converting the data transmission from high-speed USB port for example USB 2.0 (Pua's Fig 2: #2, paragraph 4) to parallel port interface for transmitting into flash memories (Pua's paragraphs 7,9). It would have been obvious to one of ordinary skill in the art at the time of invention to include the controller circuits and procedures as suggested by Pua in APA's system thereby allowing data receiving from high-speed USB port such as USB 2.0 to be distributed to various flash memory devices, thereby the high-speed transmission feature of the serial port can be fully utilized, and therefore the transmission speed can be effectively promoted (Pua's page 1 paragraph 7).

As for claim 2, the claim recites wherein the USB standard comprises the USB 2.0 standard. The claim rejected base don the same rationale as in the rejection of claim 1.

Claim 11 rejected based on the same rationale as in the rejection of claim 1.

Claim 12 rejected based on the same rationale as in the rejection of claim 2.

Claims 3,13 rejected under 35 U.S.C. 103(a) as being unpatentable over APA (US Application 10/761853), Pua et al (US2004/0255054) as applied to claims 1,11 respectively and further in view of Martwick (US 6718407).

As for claim 3, the claim recites the FLASH controller of claim 1 wherein the software program for the FLASH controller is stored along with data in at least one of the plurality of FLASH memories for cost reduction and field upgrade ability. APA does not describe the

claim's detail of storing in the flash memory. However, Martwick describes an apparatus (Fig 1: #124 self update controller) capable of dynamically storing and updating the data stored in the flash device (Martwick's Fig 4, column 3 lines 42-60). The data being stored in the flash device can be for example, data structures and programming code (column 3 lines 55-60). It would have been obvious to one of ordinary skill in the art at the time of invention to include the self update controller circuits and procedures as suggested by Martwick in APA's system that allows flash memory devices to be able to program itself easily without the need of external programming equipments normally used in the manufacturing environment (Martwick's column 1 lines 20-40).

Claim 13 rejected based on the same rationale as in the rejection of claim 3.

Claims 4-8,14-18,21-25 rejected under 35 U.S.C. 103(a) as being unpatentable over APA (US Application 10/761853), Pua et al (US2004/0255054) as applied to claims 1,12,11 respectively and further in view of Nolan et al (US 2002/0166023).

As for claims 4,6,7 the claims recites the FLASH controller of claim 1 wherein the throughput for access to a FLASH memory to match the speed of the USB standard is accomplished by providing a wider bandwidth FLASH data bus (claim 4); wherein the wider data bandwidth is provided by using a FLASH memory with the appropriate data width (claim 6); wherein the FLASH controller of claim 4 wherein the wider data bandwidth is provided by using multiple FLASH memories (claim 7). APA does not describe the claim's detail regarding using multiple flash memory devices. However, Nolan describes a memory controller (Nolan's Fig 1: #108) capable of controlling multiple memory devices (Fig 1: #122A-#122H), each device has a data width, for example 1 byte, and by using multiple devices, the memory controller can

achieve an aggregate data bus width, for example 8 bytes wide (Nolan's paragraph 14). It would have been obvious to one of ordinary skill in the art at the time of invention to include the multiple devices arrangement as suggest by Nolan in APA's system allowing greater data bandwidth by aggregating memory devices, and thereby matching the data transfer rate from the processor (Nolan's paragraph 14).

As for claim 5, the claim recites wherein the throughput for access to a FLASH memory to match the speed of the USB standard is accomplished by providing concurrent internal and external read and write cycles. APA does not describe the claim's detail of the controller with flash type detection logic. However, Nolan describes a memory controller (Fig 1: #108) capable of distributing data to multiple of memory devices (Fig 1: #122A-122H) in a pipeline manner (Fig 3).

As for claim 8, the claim recites wherein the throughput for access to a FLASH memory to match the speed of the USB standard is accomplished by providing a wider bandwidth FLASH data bus and concurrent internal and external read and write cycles. The claim rejected based on the same rationale as in the rejection of claims 4,5.

Claims 14-18,21-25 rejected based on the same rationale as in the rejection of claim 4-8 respectively.

Claims 9,19,26 rejected under 35 U.S.C. 103(a) as being unpatentable over APA (US Application 10/761853), Pua et al (US2004/0255054) as applied to claims 1,12,11 respectively and further in view of Ganton (US 2003/0163656).

As for claim 9, the claim recites including a FLASH type detection algorithm for determining if the FLASH controller supports a FLASH type. APA does not describe the claim's detail of the controller with flash type detection logic. However, Ganton describes a method and detection circuits in Fig 5: #505 serial memory interface controller, that is capable of detecting multiple flash memory device types NAND-type flash memory, ROM, EEPROM memories etc (paragraph 26,27,31-32). It would have been obvious to one of ordinary skill in the art at the time of invention to include the device type detection circuits and procedures as suggested by Ganton in APA's system to allow different data to be stored in different devices such as ROM and serial flash memory devices (Ganton's paragraphs 31-32), further optimizing the usage of different memory types thereby achieving significant cost reductions for the products (Ganton's page 2 paragraph 13).

Claims 19,26 rejected based on the same rationale as in the rejection of claim 9.

Claims 10,20,27 rejected under 35 U.S.C. 103(a) as being unpatentable over APA (US Application 10/761853), Pua et al (US2004/0255054) as applied to claims 1,12,11 respectively and further in view of North (US 2003/0046510), Grundy et al (US 2004/0148482).

As for claim 10, the claim recites the FLASH controller of claim 1 wherein an external power regulator, reset circuit and crystal are integrated via mixed signal technology or Multi-Chip package. APA does not describe the claim's detail of the integrating components. However, North describes the semiconductor technology capable of integrating reset circuit (Fig 1: #119), a calibration circuit to regulate voltage (Fig 9: # 216, paragraph 88) and crystal (paragraph 35). It would have been obvious to one of ordinary skill in the art at the time of invention to include the

integration of multiple component in a chip as suggested by North in APA's system thereby to allow to include high degree of functionality into small portable devices (North's paragraph 4). APA and North do not describe the multi-chip packaging aspect of the claim. However, Grundy describes the multi-chip package in which multiple components such as memory controller, memory devices, phase lock loop, oscillator and etc. can be assembled into one package (Grundy paragraphs 36, 107). It would have been obvious to one of ordinary skill in the art at the time of invention to include the multi-chips package method as suggested by Grundy in APA's system that greatly reduce the trace signals that travel among components (Grundy's paragraph 38), and thereby allow much higher data transfer rate paragraph 39).

Claims 20,27 rejected based on the same rationale as in the rejection of claim 10.

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2188

2/17/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER